RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2628

PATENT APPLICATION
Docket No.: 9898-176
Client Ref. No.: SS-14849-USRCERCE

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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|---|---|---|---|
| In re application of: | Dong-woo LEE et al. | | |
| Serial No.: | 09/898,699 | Examiner: | Hsu, Joni |
| Filed: | July 2, 2001 | Group Art Unit: | 2628 |
| Confirmation No.: | 2435 | | |
| For: | MEMORY DEVICE HAVING DEPTH COMPARE-WRITE FUNCTION AND METHOD FOR DEPTH COMPARE-WRITE USED BY THE MEMORY DEVICE | | |
| Date: | October 29, 2007 | | |

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## AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Final Office Action, Paper No. 62507, dated August 28, 2007, please amend the application as follows.

**Amendments to the Specification** begin on page 2 of this paper.

**Amendments to the Claims** are reflected in the listing of claims which begins on page 4 of this paper.

**Remarks/Arguments** begin on page 10 of this paper.

## IN THE SPECIFICATION

Please replace the paragraph beginning at page 2, line 21 with the following:

The memory controller compares spatial coordinate values Dout of an existing object with input spatial coordinate values Din of a new object at intervals "a". As can be seen from Fig. 1, interval "a" is two cycles long. If the input spatial coordinate values (hereinafter referred to as "external depth data") Din of the new object are smaller than the spatial coordinate values (hereinafter referred to as "internal depth data") Dout of the existing object[[.]], then [[I]]it means that the object is now closer. The memory controller then prepares for writing the external depth data Din to a memory cell array of the memory device by replacing the internal data. If there is a write command WR, then the external depth data Din standing-by in the data I/O pins DQ is written to the selected memory cell array of the memory device, in response to the write command WR.

Please replace the paragraph beginning at page 4, line 13 with the following:

Referring to FIG. 2, a memory system includes a memory device 22 according to an embodiment of the present invention, and is controlled by a memory controller 21. A monitor is not shown.

Please replace the paragraph beginning at page 4, line 19 with the following:

Furthermore, the memory controller 21 generates and transmits to memory device 22 a first control signal CS1 and a second control signal CS2 through the control pins DC0 and DC1, respectively. Control signals CS1 and CS2 may be active or non-active (implemented by choosing high and low levels). The memory controller 21 also prepares for writing external depth data through the data I/O pin DQ.

Please replace the paragraph beginning at page 6, line 3 with the following:

FIG. 4 is a timing diagram when performing a compare-record function of the memory device 22 of FIG. 3 according to an embodiment of the present invention. A depth compare-write operation of the memory device 22 is now described in detail with reference to FIGS. 3 and 4. Referring to FIGS. 3 and 4, a depth compare-write command signal WR, first and second control signals CS1 CS2, and external depth data Dw, all of which are generated by the memory

controller 21, are input into corresponding pins, i.e., a command pin (not shown), the first and second pins DC0 and DC1, and the data I/O pin DQ. This happens on the rise of the third cycle.

Please replace the paragraph beginning at page 8, line 7 with the following:

As has been described in the foregoing, according to the conventional art, at least ten clock cycles are required for one read-modify-write ("RMW") operation. However, according to an embodiment of the present invention, only six (6) or seven (7) clock cycles are sufficient for performing one RMW operation, instead of the ten (10) required in the prior art . Therefore, the invention can improve performance by more than 30% compared with the prior art.